

a substrate having a surface, a drain region, a channel region and a source region;

a trench formed in said substrate from said source region to said drain region, said trench formed vertically, essentially perpendicular to said surface of said substrate, said trench having trench walls;

a first dielectric layer formed essentially on said trench walls;

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a charge storage layer for storing charges, said charge storage layer being formed on said first dielectric layer;

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a control layer trench formed in said charge storage layer and having walls;

a second dielectric layer formed at least partially on said walls of said control layer trench and having a surface;

a control layer formed essentially on said surface of said second dielectric layer;

a trench extension formed essentially underneath said trench, said trench extension having a surface;

a third dielectric layer formed on said surface of said trench extension; and

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added*
a filler material for at least partially filling said trench extension.

Claim 2(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material is electrically isolated from said charge storage layer.

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Claim 3(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material is in electrical contact with said charge storage layer.

Claim 4(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends within said trench.

Claim 5(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends into said trench extension.

Claim 6(amended). The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer trench extends into said substrate beneath said trench extension.